
AC Line Power Factor Correction of DC Motor Drive employing Boost Converter

K. VenkateswaraRao*

E. Anil Kumar**

M. Sai Ganesh***

Abstract

With the expanding interest for control from the ac line and more stringent breaking points for control quality, control factor rectification has increased awesome consideration as of late. An assortment of circuit topologies and control techniques has been produced for the PFC application. While the intermittent conduction mode (DCM) converters, for example, help and flyback converters are appropriate for low power applications, nonstop conduction mode (CCM) support converters with normal current mode, top current mode or hysteresis control are regularly decided for some medium and high power applications. Consonant contamination and low power factor in control frameworks caused by control converters have been of awesome concern. To conquer these issues a few converter topologies utilizing propelled semiconductor gadgets and control plans have been proposed. This examination is to distinguish a minimal effort, little size, proficient and solid ac to dc converter to meet the information execution file of UPS. The execution of single stage and three stage ac to dc converter alongside different control systems are considered and thought about. This paper introduces a novel ac/dc converter in view of a semi dynamic power factor remedy (PFC) plot. In the proposed circuit, the power factor is enhanced by utilizing support dc to dc converter. It wipes out the utilization of dynamic switch and control circuit for PFC, which brings about lower cost and higher productivity. A Matlab/Simulink based model is created and reenactment comes about are introduced. At last a DC engine stack is connected and reproduction comes about are displayed.

Keywords:

AC/Dc converter;
Power factor correction;
Single stage.

Author correspondence:

K.Venkateswararao, Asst. prof, EEE dept.

* Doctorate Program, Linguistics Program Studies, Udayana University Denpasar, Bali-Indonesia (9 pt)

** STIMIK STIKOM-Bali, Renon, Denpasar, Bali-Indonesia

*** English Language Specialist, Oller Center, Carriage House, 2nd Floor, California, USA

1. Introduction

Exchanged mode Power Factor Corrected (PFC) AC-DC converters with high proficiency and power thickness are being utilized as front end rectifiers for an assortment of utilizations [1-3]. The converters are either buck or lift sort topologies. The buck sort topology gives variable yield DC voltage, which is much lower than the info voltage abundance. However when the quick info voltage is underneath the yield DC voltage, the present drops to zero that outcomes in noteworthy increment in input current THD. Indeed, even with input channels the buck converters give just constrained change in input current quality. Then again the lift sort converter dependably delivers the yield voltage higher than the info momentary voltage adequacy. The lift inductor with fitting decision keeps up constant information current with great wave shape. This lead the converter control to keep up close solidarity control factor, low information current THD and great yield voltage direction.

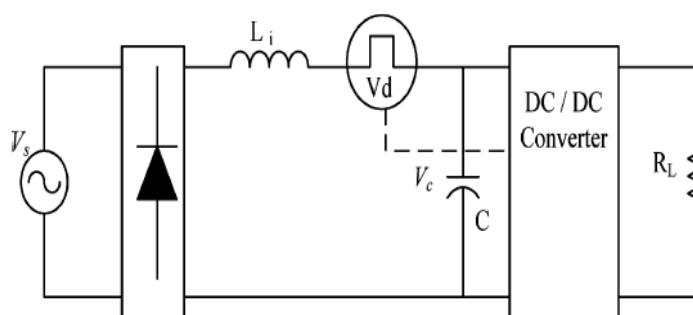


Figure 1 General circuit diagram of rectifier with PFC cell

The two-arrange plot brings about high power factor and quick reaction yield voltage by utilizing two autonomous controllers and enhanced power stages. The fundamental downsides of this plan are its generally higher cost and bigger size came about because of its muddled power arrange topology and control circuits, especially in low power applications. Keeping in mind the end goal to decrease the cost, the single-arrange approach, which coordinates the PFC organize with a dc/dc converter into one phase, is produced [1]– [11].

These coordinated single-arrange control factor adjustment (PFC) converters more often than not utilize a lift converter to accomplish PFC with irregular current mode (DCM) operation. More often than not, the DCM operation gives a lower add up to symphonious mutilation (THD) of the information current contrasted with the nonstop current mode (CCM). Nonetheless, the CCM operation yields marginally higher proficiency contrasted with the DCM operation. A definite audit of the single stage PFC converters is displayed in [3]. For the most part, single-organize PFC converters meet the administrative necessities in regards to the information current music, however they don't enhance the power factor and decrease the THD as much as their regular two-arrange partner. In this paper, another procedure of semi dynamic PFC is proposed.

As appeared in Fig. 1, the PFC cell is framed by interfacing the vitality cushion (LB) and a helper winding (L3) coupled to the transformer of the dc/dc cell, between the info rectifier and the low-recurrence channel capacitor utilized as a part of traditional power converter.

2. Active power factor correction circuit components

2.1. The fundamental principle of APFC:

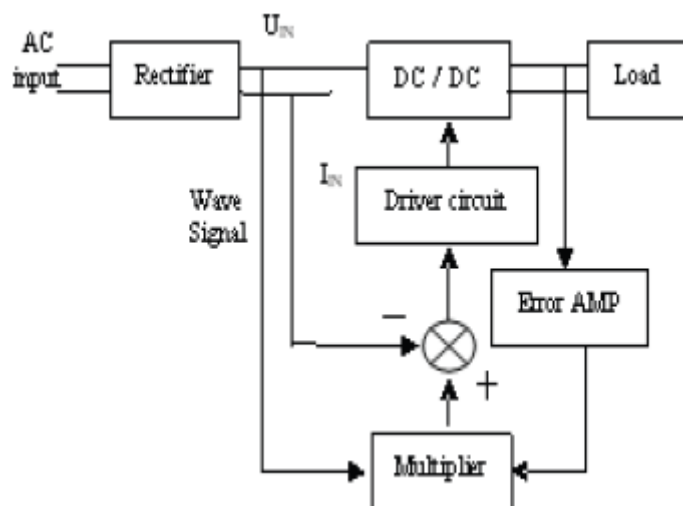


Figure 2 Basic operating principle of APFC circuit

The above Fig.2 demonstrates the working rule of APFC circuit comprises of rectifier, DC/DC converter, driver circuit, mistake intensifier and multiplier. Truth be told, APFC is implying that the rectifier voltage which the info adjust current (short for AC) flag is changed over direct-present (short for DC) voltage through the extension diode is changed into the present flag by DC to DC converter and the best possible control strategies. The present wave which would auto be able to track the DC voltage wave is changed with a sine wave, and get a consistent dc yield voltage [1]. The major guideline edge of APFC is appeared in Figure 2.

Figure1 contribution by rectifier in the wake of redressing, exchanging momentum will get sinusoidal voltage waveform motion as the information flow IC disentangles PFC reference waveform and after that by reenactment on time-multiplier operations, will get as the aftereffect of ebb and flow waveform reference, and the estimation of the ebb and flow esteem and the real examining examination, at that point in the wake of driving circuit to control flag created driver circuit DC/DC ebb and flow yield and yield voltage.

2.2. The main circuit topology of APFC:

The primary circuit topology is normally conveyed out with DC to DC converter. The principle circuit topology is comprised of buck, help buck, fly back and support circuit. Buck circuit is once in a while utilized as the enormous commotion and the terrible separating. Lift buck circuit has a multifaceted nature circuit. Fly back circuit is normally utilized as a part of low power application. The last one is a basic current control circuit as a result of the high PF esteem, the low aggregate consonant bending and the high effectiveness. The pinnacle current of lift APFC is almost equivalent to the info current. The plentifulness of the pinnacle voltage of lift APFC is higher than the framework side voltage.

3. Closed loop control of active PFC circuit

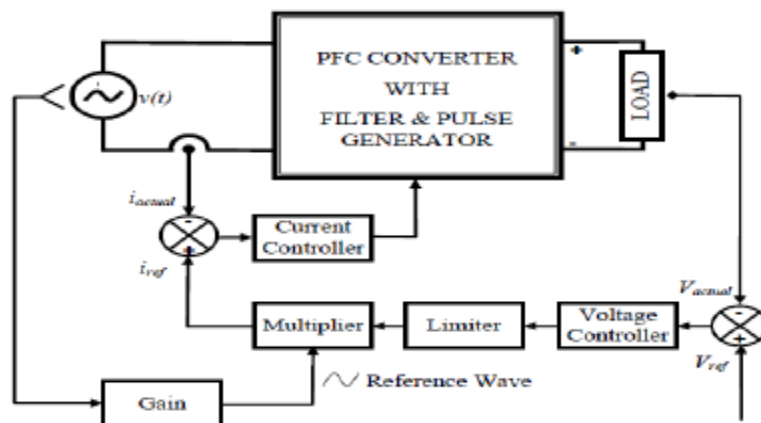


Figure 3 Closed loop control of PFC ac-dc converter

The above Figure.3 demonstrates the shut circle control for PFC air conditioning dc converter comprises of various part gadgets. The general piece chart of the shut circle control of PFC converter is appeared in Fig.3 The goal is to direct the power stream and meet the UPD input execution record, for example, yield voltage control $\leq 2\%$, input control factor ≥ 0.95 , input current bending THD $\leq 5\%$. The yield voltage is managed by the external voltage control circle. The information control factor and current wave shape are controlled by the inward current circle. Both controller are picked as PI sort compensator and spoke to by the exchange work $G_c(s) = K_p(1 + 1/T_i s)$.

Where K_p and T_i are corresponding increase and necessary time steady individually. The yield voltage is managed utilizing voltage mistake (V_{error}) acquired by looking at the deliberate real yield voltage (V_{actual}) and wanted reference voltage (V_{ref}). The V_{error} is prepared by the voltage PI-controller whose yield is the coveted current size and constrained to an outlined greatest esteem. It is increased with solidarity size sine-wave reference got from input voltage. The yield of the multiplier is the coveted sinusoidal info reference current flag (i_{ref}) with extent and stage point. This flag is additionally prepared by the direct current controller as nitty gritty in Fig.4 and produces beat width adjusted entryway heartbeats with the end goal that converter keep up input execution list.

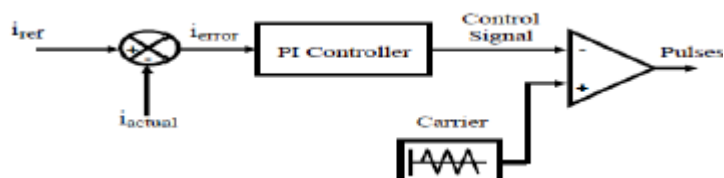


Figure 4 Linear current control

The external/voltage circle controller parameter esteems for K_p and T_i are intended to keep up steady yield voltage independent of unsettling influence because of progress in stack/input voltage.

K_p and T_i are found from open circle converter yield voltage reaction for a stage stack change [5]. While the internal/current circle controller esteems for K_p and T_i are intended to streamline PWM heartbeats to such an extent that converter operation keeps up input current close sinusoidal with constrained twisting and power factor close solidarity.

4. MATLAB/Simulink model and Simulation results

Here simulation is carried out for two cases in Case 1 AC to DC conversion without APFC is presented and in Case 2 with APFC are presented.

4.1. AC to Dc converter without APFC:

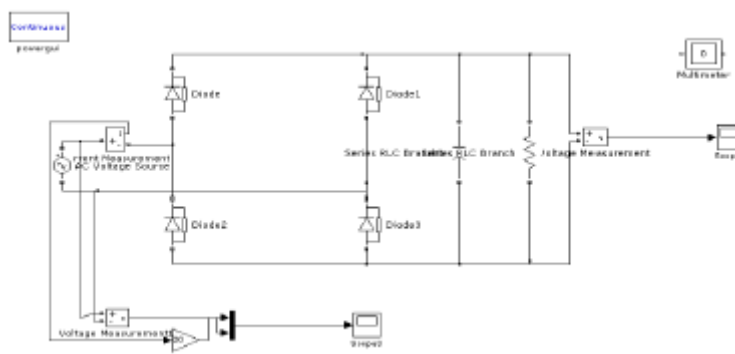


Figure 5 Matlab/Simulink model without APFC

The above figure demonstrates the essential rectifier circuit with capacitor over the R-heap of simulink document without APFC.

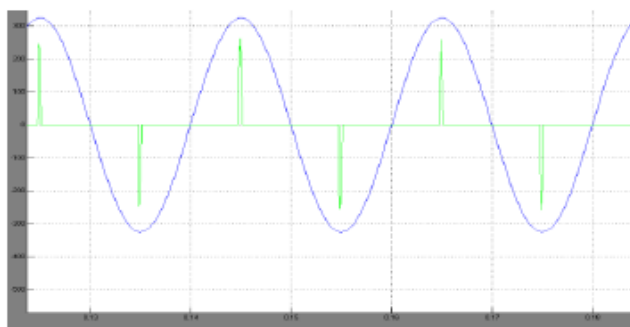


Figure 6 Voltage and current waveforms of input supply side power factor

The above figure shows AC side voltage and current waveforms without APFC.

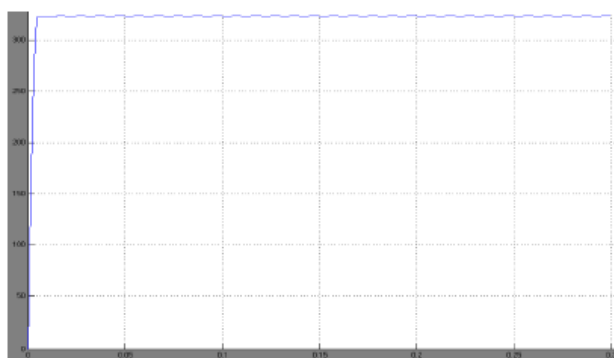


Figure 7 the constant output dc voltage at the load side waveform

The above figure shows Output DC voltage without APFC simulink model.

4.2. AC to Dc converter with APFC:

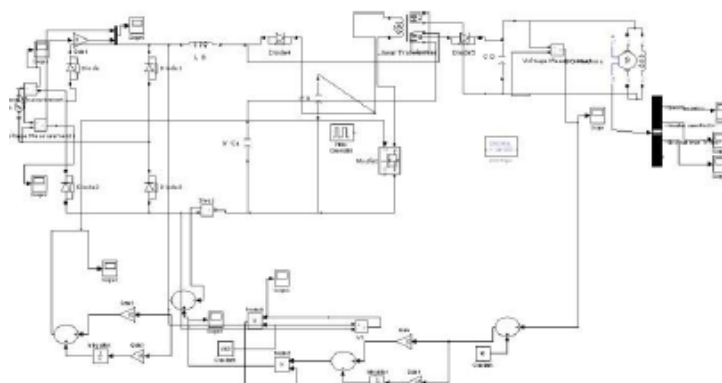


Figure 8matlab/Simulink model with APFC

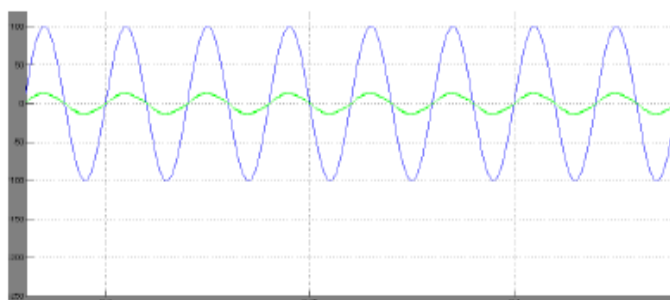


Figure 9the input voltage and current in phase with voltage of unity power factor

The above figure shows AC side voltage and current waveforms with APFC simulink model.

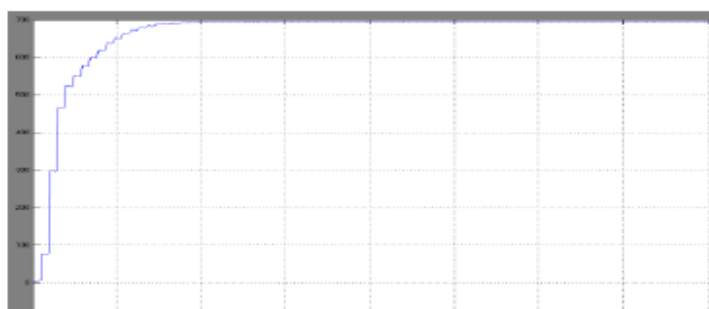


Figure 10constant output Dc voltages at the load side with APFC

The above figure shows Output DC voltage constant with APFC simulink Model

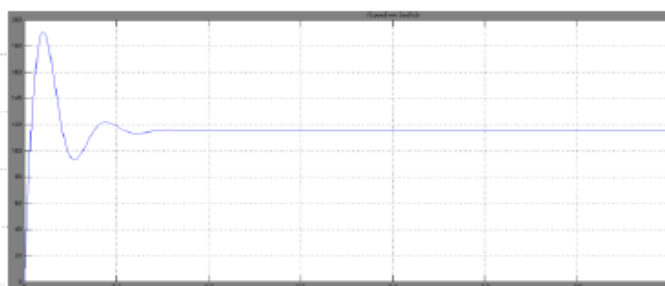


Figure 11dc motor speeds in rad/sec with APFC Simulink output

The above figure shows the DC motor speed in rad/sec with APFC simulink model

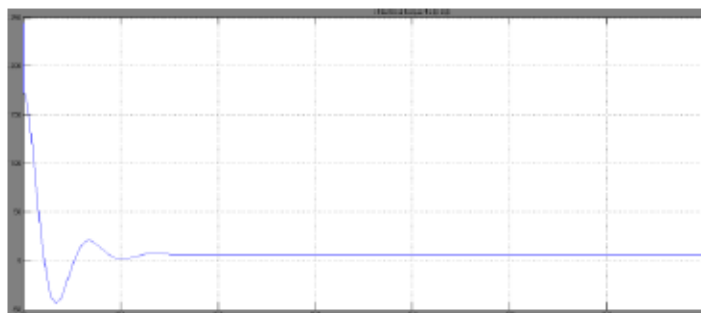


Figure 12 dc motor torque in N-m

The above Figure shows the DC motor Torque in N-m with APFC simulink model

5. Conclusion

In this paper, another air conditioner/dc converter in view of a semi activePFC conspire has been exhibited. The proposed technique creates a current with low consonant substance to meet the standard details and additionally high productivity. This circuit depends on adding a helper twisting to the transformer of a course dc/dc DCM flyback converter. The proposed converter is connected to a dc engine drive. At last a Matlab/Simulink based model is produced and reproduction comes about are displayed.

References

- [1] Hussain S. Athab, Dylan Dah-Chuan Lu|| A High- Efficiency AC/DC Converter With Quasi-Active Power Factor Correction|| Eee Transactions On Power Electronics, Vol. 25, No. 5, May 2010, P.P 1103-1109.
- [2] R. Redle, L. Balogh, and N. O. Sokal, —A new family of single-stage isolated power factor correctors with fast regulation of the output voltage, in *Proc. IEEE PESC 1994 Conf.*, pp. 1137–1144.
- [3] C. Qian and K. Smedley, —A topology survey of single-stage power factor with a boost type input- current-shaper,||*IEEE Trans. Power Electron.* vol. 16, no. 3, pp. 360–368, May 2001.
- [4] T.-F. Wu, T.-H. Yu, and Y.-C. Liu, —An alternative approach to synthesizing single-stage converters with power factor correction feature,||*IEEE Trans. Ind. Electron.*, vol. 46, no. 4, pp. 734 748, Aug.1999.
- [5] L. Huber, J. Zhang, M. Jovanovic, and F.C. Lee, Generalized topologies of single-stage input-current- shaping circuits,|| *IEEE Trans. Power Electron.*, vol. 16, no. 4, pp. 508–513, Jul. 2001.
- [6] Wei, I. Batarseh, G. Zhu, and K. Peter, —A single- switch ACDC converter with power factor correction,|| *IEEE Tran Power Electron.*, vol. 15, no. 3, pp. 421–430, May 2000.
- [7] L. K. Chang and H. F. Liu, —A novel forward AC/ converter with input current shaping and fast output voltage regulation via reset winding,|| *IEEE Trans. Ind. Electron.*, vol. 52, no. 1, pp. 125–131, Feb. 2005.
- [8] H. L. Do, —Single-stage single-switch power factor AC/DC converter,||*Inst. Electr. Eng. Proc. Electr. Power Appl.*, vol. 152, no. 6, pp. 1578–1584, Nov. 2005.
- [9] J. Qian, Q. Zhao, and F. C. Lee, —Single-stage single- switch power factor correction ac/dc converters with dc-bus voltage feedback for universal line applications,|| *IEEE Trans. Power Electron.*, vol. 13, no. 6, pp. 1079–1088, Nov. 1998.
- [10] S. Luo, W. Qiu, W. Wu, and I. Batarseh, —Flyboost power factor correction cell and a new family of single-stage AC/DC converters,|| *IEEE Trans. Power Electron.*, vol. 20, no. 1, pp. 24–33, Jan. 2005.
- [11] M. M. Jovanovic, D. M. Tsang, and F. C. Lee, Reduction of voltage stress in integrated high- quality rectifiers-regulators by variablefrequency control,|| in *Proc. IEEE APEC 1994 Conf.*, pp. 569– 575.
- [12] J. Sebastian, A. Femandez, P. Villegas, M. Hemando, and J. Prieto, —New topologies of active input current shapers to allow AC-to-DC converters with asymmetrically driven transformers to comply with the IEC-10003-2,|| *IEEE Trans. Power Electron.*, vol. 17, no. 4, pp. 493–501, Jul.2002.
- [13] N. Vazquez, J. Lopez, J. Arau, C. Hernandez, and Elias Rodriguez, —A different approach to implement an active input current shaper,|| *IEEE Trans. Ind. Electron.*, vol. 52, no. 1, pp. 132–138, Feb. 2005.
- [14] K. Zhou, J. G. Zhang, S. Yuvarajan, and D. F. Weng, Quasiactive power factor correction circuit for switching power supply,||. O. Gracia, J. A. Cobos, R. Prieto, and J. Uceda.

